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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,238	10/21/2003	Minakshisundaran B. Anand	YOR920030315US1	4930

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/690,238	ANAND ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/690,238, and Amendment filed on 10/21/2005. Independent claim 1 has been amended by including additional limitations. Claims 1-28 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being unpatentable Chang et al. (US Patent 5,610,833).

As to claim 1 Chang discloses:

A computer aided design (CAD) system for designing high performance circuits, said CAD system comprising (col.4, ll.40-67):

a graphical user interface (GUI) (a spreadsheet-style graphical user interface-col.3, l.48) having input fields (fig. 1b) including conductor and dielectric input fields (the construction worksheet 530 comprises a plurality of spreadsheet cells 532, 534, 536 containing data relating to electrical and physical characteristics of different parameters of a particular chip construction-col.13, 15-18; table 5 lists preferred data types and units for each column-col.13, ll.21-39) (col.3, ll.34-55; col.4, ll.25-26; col.5, ll.1-24; col.13, ll.3-39);

a template generation engine interfaced with said GUI and generating multidimensional templates (Four subsystems are integrated: (a) a batch-mode computation module that combines a 2-D/3-D finite difference numerical simulation and a fast interpolation algorithm ... and (d) a spreadsheet-style graphical user interface-col.3, ll.40-48) from interconnect configuration files (data processing methods receive input of layout parameters and technology parameters identifying the circuit to be designed-col.5, ll.5-7); (col.3, ll.34-55; col.5, ll.1-15; col.5, ll.25-28) and

a field solver (SPICE Subcircuit Generator ... control is passed to step 220 in which the invention will generate a SPICE deck or file for the interconnect being analyzed – col.16, ll.6-11) using conductor and dielectric inputs (the construction worksheet 530 comprises a plurality of spreadsheet cells 532, 534, 536 containing data relating to electrical and physical characteristics of different parameters of a particular chip construction-col.13, 15-18; table 5 lists preferred data types and units for each column-col.13, ll.21-39) to determine circuit interconnection electric parameters (in step 220, the method of the invention causes a data processor to read the equation file 406 and generate parameterized three-line circuit models for distributed R,C circuit simulation – col.16, ll.36-39) (col.3, ll.55-62; col.8, ll.26-40; col.13, ll.3-39; col.14, ll.41-51; col.16, ll.6-15; col.16, ll.36-54).

As to claim 2 Chang teaches:

A CAD system as in claim 1, wherein said input fields are geometric and property specification input fields (col.12, ll.40-67; col.13, ll.1-39).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3-28 are rejected under 35 U.S.C. 103(a) as being unpatentable by Meuris et al. (US Patent 6,665,849) in view of Chang.

4. As to claims 3 and 15 Meuris recites:

(3) A computer aided design (CAD) system comprising (Abstract):

a field solver generating broadband passive element relationships (passive structures) from said templates (col.38, ll.13-67; col.39; col.40, ll.1-63);

a circuit builder (structure generator) generating circuit description files (data structures/files) from device technology models and said broadband passive element relationships (col.28, ll.19-67; col.29, col.30; col.31, ll.1-19; col.41, ll.44-67; col.42, ll.1-15; col.44, ll.8-58); and

a simulator simulating circuit responses for transmission line models from said circuit description files (col.24, ll.18-67; col.25, ll.1-21; col.41, ll.44-67; col.42, ll.1-15; col.44, ll.59-67);

(15) A CAD system for designing high performance circuits, said CAD system comprising (Abstract):

a graphical user interface (GUI) having input fields including conductor and dielectric input fields (col.14, ll.51-67; col.15; col.16, ll.1-28; col.22, ll.40-46; col.32, ll.4-11; col.44, ll.9-29);

a field solver using produced interconnect structure and the electromagnetic boundary conditions to determine interconnection structure parameters (col.5, ll.33-67; col.6, ll.45-65; col.9, ll.59-67; col.38, ll.44-65).

With respect to 3-28 Meuris teaches the features above but lacks a computer aided design system further comprising a template generation engine generating templates from interconnect configuration files.

5. As to claims 3 and 15 Chang in view of Meuris discloses:

A computer aided design (CAD) system for designing high performance circuits, said CAD system comprising (col.4, ll.40-67):

a template generation engine generating templates (Four subsystems are integrated: (a) a batch-mode computation module that combines a 2-D/3-D finite difference numerical simulation and a fast interpolation algorithm - col.3, ll.40-48) from interconnect configuration files (data processing methods receive input of layout parameters and technology parameters identifying the circuit to be designed-col.5, ll.5-7); (col.3, ll.34-55; col.5, ll.1-15; col.5, ll.25-28).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Chang's teaching regarding the computer aided design system further comprising a template generation engine generating templates from interconnect configuration files and use it in Meuris' invention to improve a data

processing system for interconnect modeling, thereby improving an efficiency of the high-speed chip designs.

6. As to claims 4-14 and 16-28 Meuris in view of Chang teaches:

(16) A CAD system, wherein said input fields are geometric and property specification input fields (col.44, ll.8-29);

(4) A CAD system as in claim 3, further comprising a geometry and material definition module receiving process description and generating said interconnect configuration files (col.14, ll.511-67; col.15, ll.1-56; col.44, ll.8-29);

(5), (6), (14) A CAD system, wherein process inputs are varied in said process description through a graphical user interface (GUI) (col.15, ll.57-67; col.16, ll.1-28);

(7), (8), (17), (18), (20), (24), (25) A CAD system, wherein said interconnect configuration tiles include two dimensional inductance templates and three-dimensional templates for interconnect wiring layers (col.7, ll.40-67; col.8, ll.1-23; col.20, ll.6-54; col.38, ll.44-58);

(9), (11), (21), (26) A CAD system, wherein said 2D and 3D capacitance templates provide multiple dielectric stack inclusion (col.22, ll.40-67; col.23; col.24, ll.1-16; col.38, ll.44-58);

(10), (22), (27), (28) A CAD system, wherein said broadband passive relationships include frequency dependent resistance and inductance (col.7, ll.40-67; col.8, ll.1-23; col.19, ll.13-33; col.20, ll.6-53; col.38, ll.44-58; col.44, ll.59-67);

(12), (13) A CAD system, wherein said template generation engine generates two dimensional (2D) broadband inductance templates for lines in a first layer and in at

least each of a layer above and below said first layer (col.20, ll.6-54; col.38, ll.44-67; col.39; col.40, ll.1-62);

(19) A CAD system, wherein said 2D capacitive representation further includes a conductance representation of dielectric properties (col.6, ll.53-62);

(23) A CAD system, wherein the frequency dependent inductance effects include skin effects, proximity effects and return path proximity effects (col.4, ll.7-47; col.13, ll.40-64).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N L

Thuan Do
Primary examiner.
12/09/08